neuroSoC

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NeuroSoC HORIZON EUROPE Project:

A multiprocessor System-on-Chip with In-Memory neural processing unit

A 42-month EU/UKRI/Switzerland funded project aiming at using Phase Change Memory and FD-SOI 28 nm technologies to develop an advanced multiprocessor System-on-Chip

The project involving 12 partners from 9 countries was officially launched on September 1, 2022.

About the project

Deployment of Artificial Intelligence (AI) at the edge presents many challenges as devices are resource constrained in terms of memory and computation capacity, and must have a low power consumption profile while also being low cost. These constraints are becoming increasingly difficult to meet as advanced AI algorithms require Megabytes of storage and tens of billions of operations per second.

Hardware acceleration technologies based on neuromorphic and in-memory computing architectures have the potential to deliver a quantum leap in computational efficiency for AI applications.

The NeuroSoC project will design and demonstrate an advanced Multiprocessor System-on-Chip based on Phase Change Memory (PCM) technology targeting a 100-fold Improvement in computational efficiency, enabling an industry-proven path to bring AI to the edge.

NeuroSoC consortium partners will build upon their unique and rich portfolio of expertise in PCM, a non-volatile nanoscale memory technology that can be adapted for analog in-memory computing architectures.

The NeuroSoC advanced Multiprocessor System-on-Chip prototype will be developed in FD-SOI 28nm CMOS technology and will integrate an analog In-Memory Neural Processing Unit (IMNPU), a local digital processing subsystem, and functionally safe multiprocessor host subsystems based on an enhanced version of existing RISC-V microprocessor implementation. Covering IMNPU security aspects holistically will enable NeuroSoC to tackle the requirements of a wide set of edge-AI applications.

The In-Memory Neural Processing Unit (IMNPU) and associated digital peripheral circuitry will obviate the need to shuttle around millions of model parameters when running AI workloads such as deep neural networks (DNNs), greatly enhancing compute efficiency well beyond what purely digital solutions can achieve in traditional architecture.

The architecture developed will be scalable, configurable, and parametric, in order to provide a hardware substrate that can target a variety of applications and can support a tradeoff between the capabilities, the size of the chip, the costs and the power consumption.

The NeuroSoC consortium is a close-knit network of large groups (STM, IBM, BOSCH), SMEs (BENKEI and UBOTICA), Universities and Research centers (Leiden University, Patras University, Pavia University, Bologna University, SCCH, ETH Zurich and Kings College of London).

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Funded by the European Union

The NeuroSoC project is funded under Horizon Europe Grant Agreement n° 101070634

UKRI Innovate UK

At a glance

Acronym: NeuroSoC

Title: A multiprocessor System-on-Chip with In-Memory neural processing unit

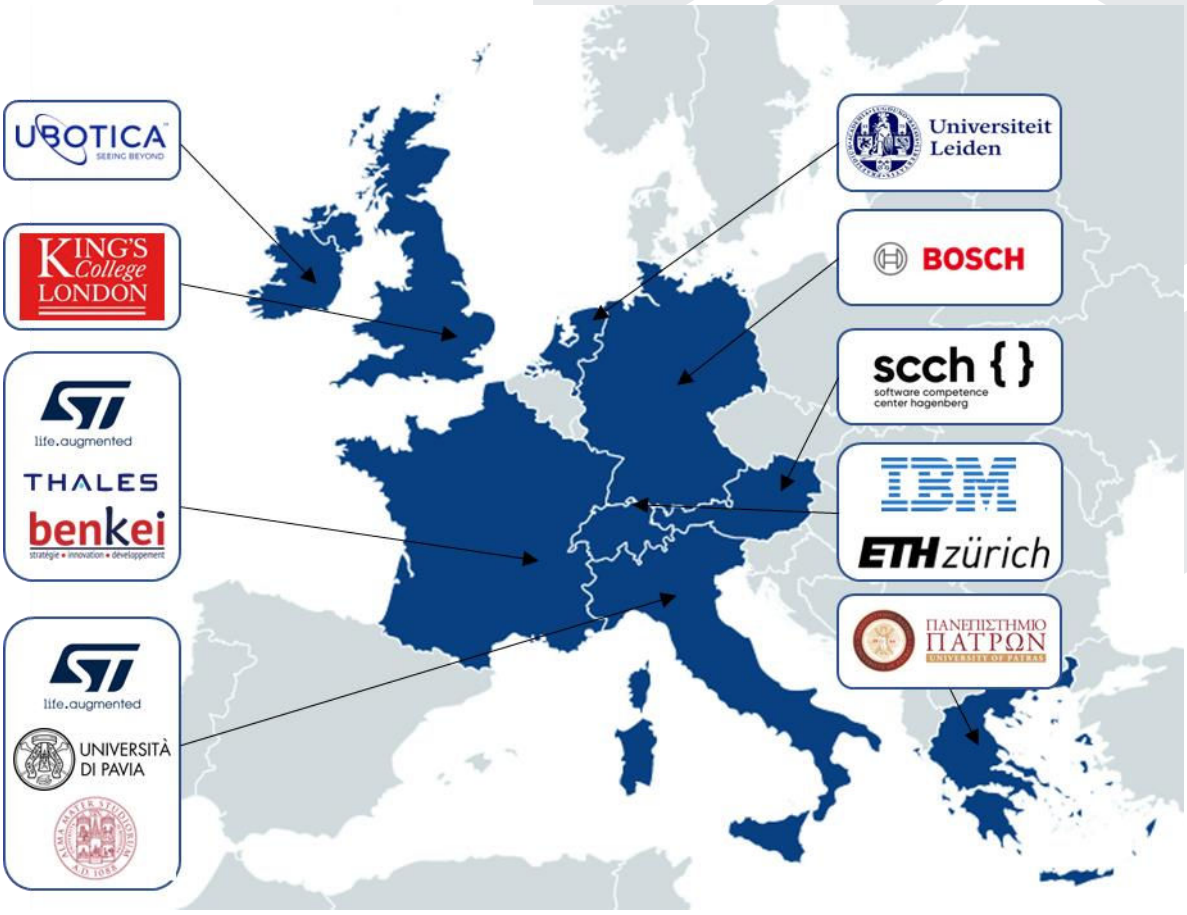
Call Identifier: HORIZON-CL4-2021-DIGITAL-EMERGING-01-01 — Ultra-low-power, secure processors for edge computing (RIA)

GA number: 101070634

Project cost: 7 952 677,50 EUR (only beneficiaries)

Duration: 42 months; start 1 September 2022

Beneficiaries: 10 beneficiaries – 1 affiliated entity – 3 associated partners



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