neuroSoC

About NeuroSoC

Public presentation

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This work was supported by European Union (Horizon Europe Grant Agreement n°101070634), Swiss State Secretariat for Education, Research and Innovation (SERI) under contracts number SBFI 22.00202 and 23.00205 and UK Research and Innovation (UKRI) under the UK government's Horizon Europe funding guarantee [grant number 10040829]

About NeuroSoC

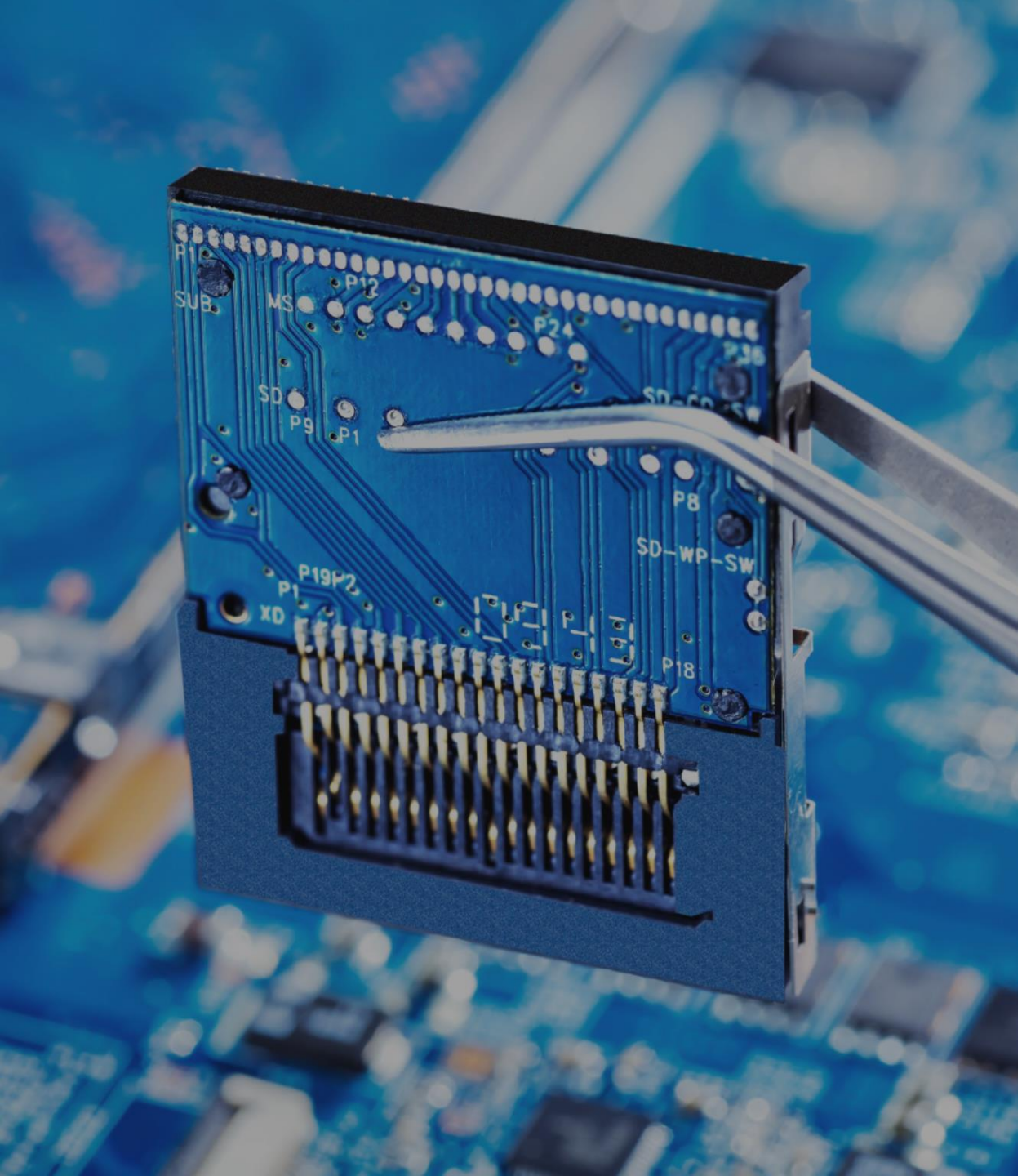
NeuroSoC stands for:

A multiprocessor System-on-Chip with In-Memory neural processing unit

A 42-month EU/UKRI/Switzerland funded project aiming at using Phase Change Memory and FD-SOI 28 nm technologies to develop an advanced multiprocessor System-on-Chip

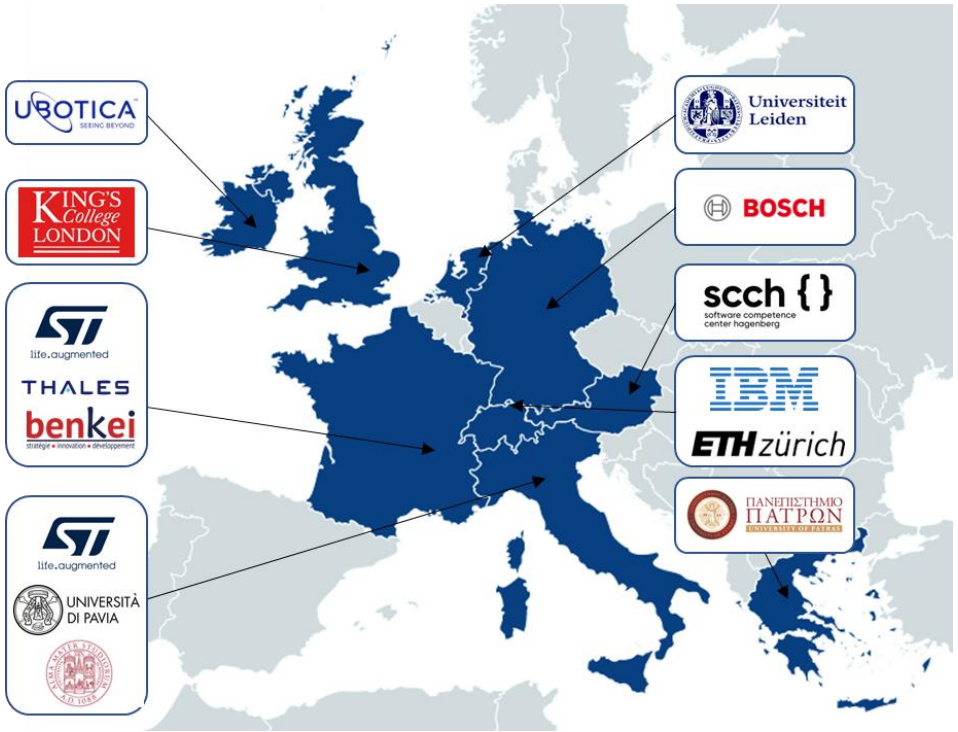
NeuroSoC at a glance

Call and Topic/Activity:	HORIZON-CL4-2021-DIGITAL-EMERGING-01-01 — Ultra-low-power, secure processors for edge computing (RIA)
GA number:	101070634
Type of action:	RIA (Research & Innovation Action)
Project cost:	7 952 677 EUR (only beneficiaries)
Duration:	42 months; start 1 September 2022
Website:	www.neurosoc.eu



Chapter 01

An european strong value chain



NeuroSoC Rationale

- The explosive growth of artificial intelligence and its movement to the edge and end devices have prompted significant research on **highly energy efficient and low-latency non-von Neumann computing paradigms such as in-memory computing (IMC)**

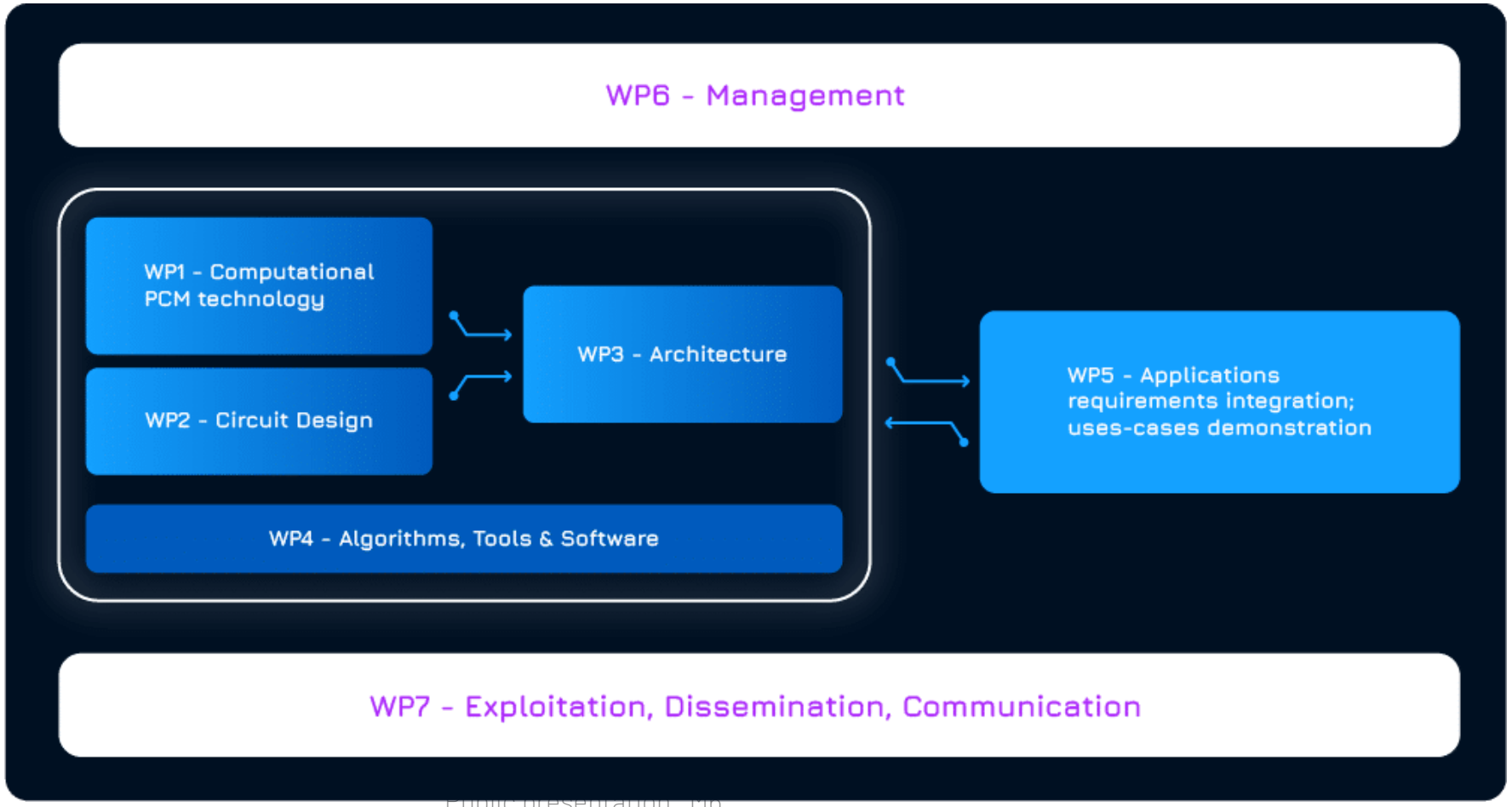
neuroSoC answer

- The overarching objective of NeuroSoC is to develop a **flexible computing system where an analog IMC-based neural processing unit** is integrated into a **multi-processor functional safe and secure system-on-chip** to tackle the requirements of a wide set of edge-AI applications.
- The NeuroSoC approach is relying on a **solid, mature, and qualified reliable Phase Change Memory** technology, that will enable to create an industrially proven path answering to the level of maturity need compatible with a mass volume production and cost.

Project structure

7 Workpackages among which

- 5 technical ones
- 1 dedicated to management
- 1 dedicated to communication, dissemination and exploitation



Workpackage 1 - Computational PCM technology

Leader: IBM

- Characterization and modelling of a Phase Change Memory (PCM) device developed by ST-I in FD-SOI 28nm technology to serve as the building block of the In-Memory Computing (IMC) tile.
  - Programming optimization to desired analog conductance values.
  - Accurate compact models' development to facilitate the design of the IMC tiles in WP2.
  - Statistical models' development based on array-level characterization,
  - Evaluation of the overall compute precision based on the conductance fluctuations and other non-idealities associated with these devices.

Workpackage 2 - Circuit design

Leader: ETHZ

- Leveraging the multilevel PCM device to design an analog IMC tile.
  - Definition of the unit cell and a suitable array structure.
  - Design of the associated digital and analog circuits
  - Anticipate inputs from security analysis to make the resulting IMC tile more robust against side channels attacks and for improved security.

Workpackage 3 - Architecture

Leader: ST-Italy

- Design of a modular IP implementing a Neural Processing Unit (NPU) with a hybrid digital and analog computational model.
  - Demonstration of a design-time parametric IP supporting multi-tile implementations and scalable from ultra-low cost and power applications.
  - Integration in a Multi-Processor System on Chip (MPSoC) system level architecture.
  - Development and integration of an enhanced version of a RISC-V microprocessor core.

Workpackage 4 - Algorithms, Tools & Software

Leader: SCCH

- Development of software extensions, primitives, deployment tools and customized algorithms to fully exploit the NeuroSoC system-level architecture.
  - Exploration of novel Instruction-Set Architecture (ISA) extension techniques.
  - Development of vertically integrated deployment flows targeting both IMNPU-based and software-based computation.
  - Mapping use-cases and investigating strategies to exploit the whole NeuroSoC system-level architecture.

Workpackage 5 - Applications requirements, integration, and use- cases demonstrations

Leader: UBOTICA

- Investigate edge-applications where NeuroSoC can offer a compelling advantage.
  - Selection and qualification of applications.
  - Benchmarking of SoA and emerging solutions.
  - Proposition of an evaluation framework.
  - Assessment.

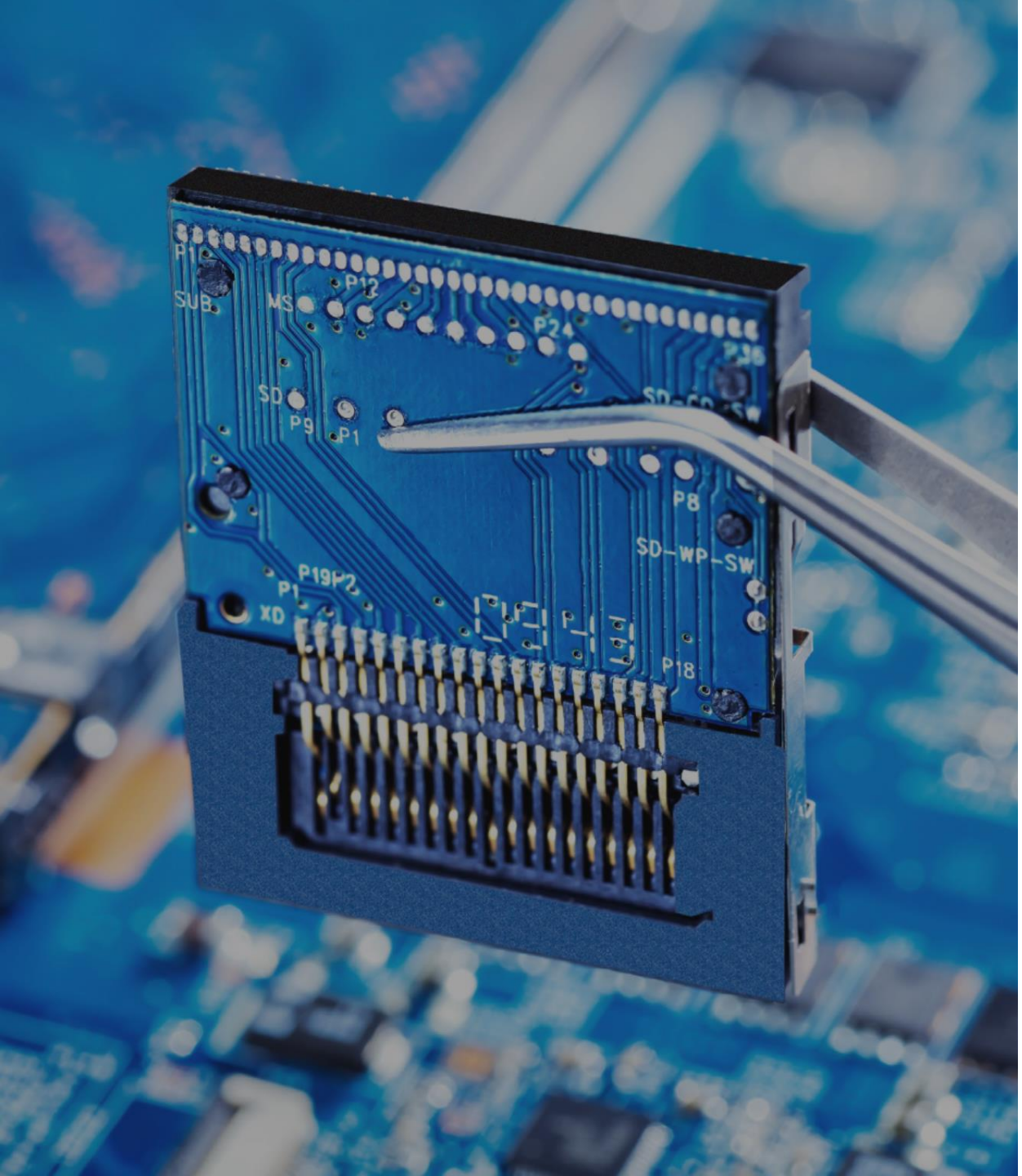
NeuroSoC objectives

- Design of a PCM computational memory tile for AIMC in 28nm FD-SOI technology
- Design of a SRAM computational memory tile for AIMC in 28nm FD-SOI technology complementing the PCM one for selected ultra-low cost and always on use-cases
- Design of a reusable and modular hybrid IMC based neural processing unit for scalable edge-AI SoCs
- Assessment and characterization of security exploits techniques for IMC based NPUs
- Enhancement of a RISC-V multicore microcontroller implementation to support functional safety
- Explore functional safety solutions for IMNPU IPs for industrial and automotive use cases
- Study and optimize AI Deep Learning algorithms optimized for IMC and selected use-cases
- Prototype IMC based AI tools and compilers for efficient mapping of deep learning algorithms
- Design of an advanced 28nm FD-SOI complete MPSoC integrating the technology developed in the project
- Validate use-cases to assess the benefits of the technology and tools developed in the project

Public deliverables

(will be made available on www.neurosoc.eu and zenodo)

- Competitors, benchmarks and KPIs report (WP5)
- RISC-V co-processor unit for IMNPU specifications, functional safe RISC-V host core specifications (WP3)
- Tool-flow for performance evaluation (WP5)
- Report on AI optimized ISA extensions (WP4)
- Methodology for off-line IMC optimized ISO accuracy training (WP4)
- Porting of Linux on the emulated RISC-V host multiprocessor (WP4)
- Final report on data converters (WP2)



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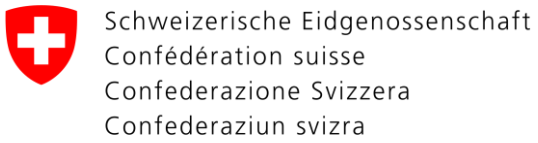

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