neuroSoC

PRESS RELEASE / MARCH 2024

NeuroSoC HORIZON EUROPE Project:

A multiprocessor system on chip with in-memory neural processing unit

A 42-month EU/UKRI/Switzerland funded project aiming at using Phase Change Memory and FD-SOI 28 nm technologies to develop an advanced multi-processor System-on-Chip

Main achievements after 12 months of work

In the first year of the project, the focus of the work has been the ***definition of the hardware architecture*** and the various elements needed, with a special focus on the ***development of a PCM NVM memory*** capable to store multilevel values, and to perform In Memory Computing.

- For the IMNPU unit, ***three distinct architectures***, namely the router-based, cluster-based and 2D mesh-based architectures, were evaluated for their suitability for the targeted weight stationary system. More specifically, the architectures were assessed for design flexibility, scalability, performance/cost and power efficiency. Finally, the 2D mesh-based architecture was selected as a suitable candidate for NeuroSoC. Various approaches to schedule the data processing in the mesh architecture have been discussed with the conclusion that two schemes, the time scheduling approach and the data driven approach provide advantages for specific use cases. The evaluation of these approaches brought the conclusion that ***both approaches seem to have their advantages and disadvantages***. Since the implementation of the required hardware support for both schemes is negligible, we decided to support both schemes and to provide the software tool chain with the freedom to use one or the other depending on the use case and better applicability. ***The initial version of the RISC-V component*** has been synthesized in various configurations.
- Regarding the security aspects, two methods, the ***"Encoder-Decoder based approach" and the "Tile-by-Tile approach"*** have been successfully explored, showing potential security risks on the In-Memory Computing (IMC) based systems due to Side-Channel Attacks.
- For the characterization of the PCM cell, a set of different type of cells have been considered, and two batches of standard and rheostatic cells have been fabricated and extensively characterized. On these cells, **a *multilevel programming algorithm*** has been implemented. With the results obtained in the first period, the multilevel is working, but convergence is not always guaranteed. The algorithm and the convergence are under refinement. The computational accuracy of the Analog In Memory Computing based on PCM, and the comparison with the digital compute engine are under evaluation.
- For the design of the AIMC tile, two architectures have been considered, ***one main architecture and one exploratory architecture***, both starting from elements of existing tiles from IBM and ST.
- ***A RTL design of the AIMC tile***, to be integrated in the overall architecture, has been realized, and it is ready to be produced for the verification of the real hardware.
- For the AIMC based on SRAM, ***a first test chip*** has been realized and it is currently under evaluation in terms of non-idealities of the real hardware and effect of analog noise sources.
- Finally, *a* ***first version of the wrapper of the AIMC tiles*** in the main architecture has been defined.
- Regarding the development of the software toolchain to be used to program the NeuroSoC system, based on the hardware architecture that has been depicted during the first year, ***the software stack components*** have been identified and connected in a proper structure, in order to allow the deployment of neural networks on the emulator first, and finally on the NeuroSoC device. In the first year the focus has been on the definition of the software architecture and the related simulations/emulation elements, taking into consideration the needs of the end user for the demonstration of efficiency and quality level requirements.

Based on the variety of applications considered, from automotive to aerospace, security and safety, the requirements of the target applications of the NeuroSoC device have been analyzed and the ***possibility of fulfillment of these requirements with the defined architecture has been confirmed.***

Funded by the European Union

Innovate UK

Schweizerische Eidgenossenschaft
Confédération suisse
Confederazione Svizzera
Confederaziun svizra

This project is supported by European Union (Horizon Europe Grant Agreement n°101070634), Swiss State Secretariat for Education, Research and Innovation (SERI) under contracts number SBFI 22.00202 and 23.00205 and UK Research and Innovation (UKRI) under the UK government's Horizon Europe funding guarantee [grant number 10040829]

PRESS RELEASE / MARCH 2024

Contact details

M. Giulio Urlini, Project Coordinator, STMicroelectronics (giulio[dot]urlini[at]stmicroelectronics[dot]com)

Mrs Fabienne Brutin, Project administrative manager, Benkei (fabienne[at]benkei[dot]eu)

At a glance

Acronym: NeuroSoC

Title: A multiprocessor system on chip with in-memory neural processing unit

Call Identifier: HORIZON-CL4-2021-DIGITAL-EMERGING-01-01

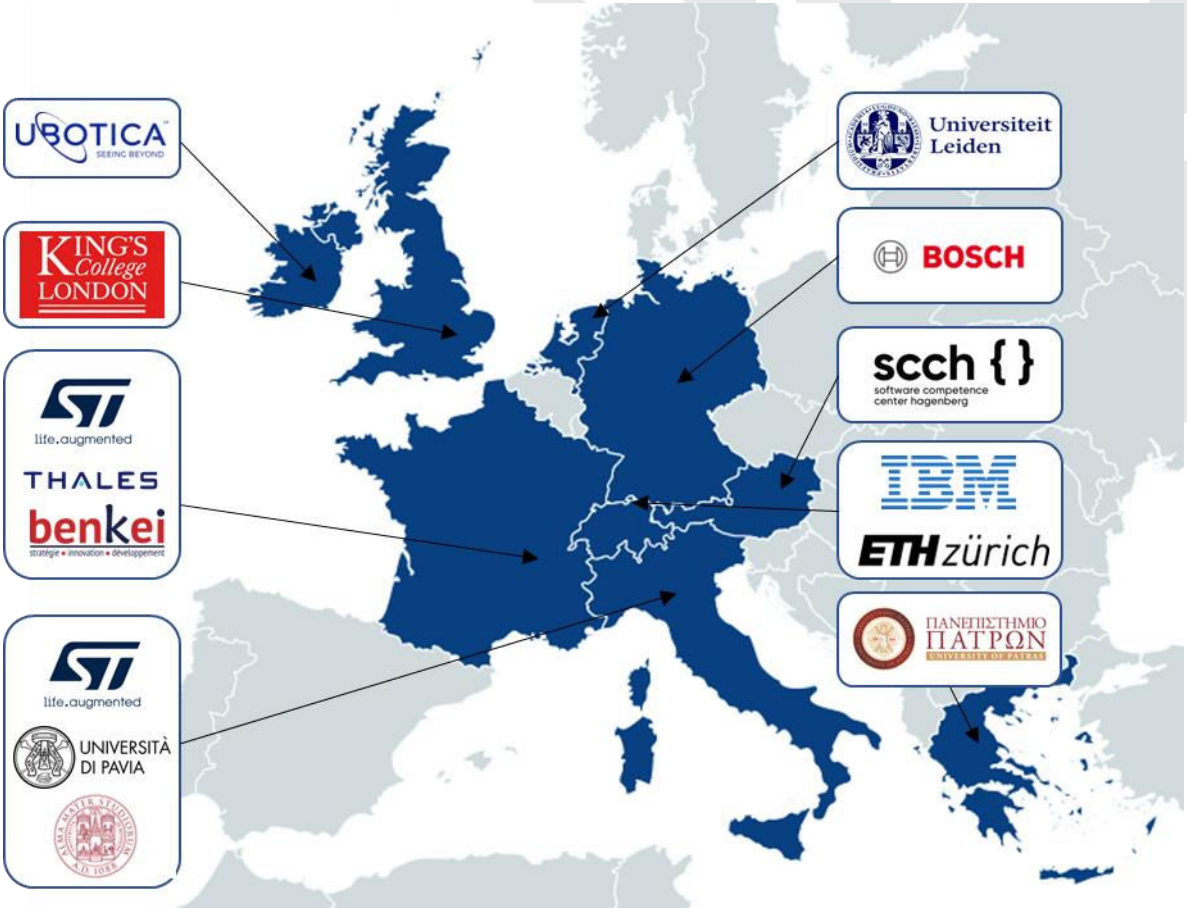
Ultra-low-power, secure processors for edge computing (RIA)

GA number: 101070634

Project cost: 7 952 677,50 EUR (EU beneficiaries only)

Duration: 42 months; start 1 September 2022

Beneficiaries: 10 EU beneficiaries – 1 affiliated entity – 3 associated partners (UK, CH)



Funded by the European Union

Innovate UK

Schweizerische Eidgenossenschaft
Confédération suisse
Confederazione Svizzera
Confederaziun svizra

This project is supported by European Union (Horizon Europe Grant Agreement n°101070634), Swiss State Secretariat for Education, Research and Innovation (SERI) under contracts number SBFI 22.00202 and 23.00205 and UK Research and Innovation (UKRI) under the UK government's Horizon Europe funding guarantee [grant number 100408291